REMARKS

Filed concurrently hereto is a Petition and fee for a two-month extension of time and an RCE. Various claims have been amended to more accurately reflect the wording in the specification concerning the embodiment shown in Figure 4 and relevant explanation in the specification. In a telephone interview with Examiner Li dated August 1, 2006, having reviewed a previously-sent copy of these claim amendments, the Examiner indicated that these claim amendments would raise new issues. Therefore, to expedite prosecution, Applicant concurrently files an RCE, rather than filing an After Final Amendment.

Claims 1-35 are all the claims presently pending in this application.

It is noted that Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 19-35 are allowed.

Claims 1, 2, 4-16, and 18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over US Patent 5,923,892 to Levy, further in view of U.S. Patent No. 4,860,200 to Holmbo. Claim 3 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Levy/Holmbo, further in view of Irwin (U.S. Patent No. 4,695,945). Claim 17 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Levy/Holmbo, further in view of Yamanaka (U.S. Patent No. 4,774,625).

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

As described in, for example, claim 1, the claimed invention is directed to a microprocessor system for executing instructions described in a program. The system includes a main processor executing, by hardware, instructions which belong to a first instruction set and executing, by software, instructions which belong to a second instruction set. The main processor includes an interrupt request reception circuit to encode an interrupt vector for the execution of an instruction of the second instruction set by using an interrupt handler, and the interrupt request reception circuit generates an interrupt vector address corresponding to the interrupt vector.

A co-processor is operative under the control of the main processor and autonomously fetches an instruction belonging to the second instruction set to execute same by hardware of the co-processor. The co-processor includes an interrupt request generation circuit for decoding an interrupt request signal. The interrupt request generation circuit is connected to the interrupt request reception circuit by at least one signal line. The decoding allows the interrupt vector address to be identified in the main processor.

II. THE PRIOR ART REJECTIONS

As recited in amended claim 1, the interrupt request generation circuit provided in the co-processor decodes the interrupt request signal, generates the interrupt vector, and outputs the interrupt vector to the interrupt request reception circuit provided in the main processor. Upon receipt of the interrupt vector, the interrupt request reception circuit generates the interrupt vector address corresponding to the interrupt vector thus received. At this time, the decoding by the interrupt request generation circuit allows the interrupt vector address to be identified in the main processor. As a result, the interrupt request reception circuit can generate an interrupt address corresponding to the received interrupt vector immediately.

In contrast, Levy and Holmbo fail to disclose or suggest the structure of the present invention. Therefore, the present invention is not obvious from Levy or Holmbo. The Examiner relies upon Irwin and Yamanaka for reasons unrelated to this deficiency.

Hence, turning to the clear language of the claims, in Levy and/or Holmbo, there is no teaching or suggestion of: "A microprocessor system for executing instructions described in a program, said system comprising: a main processor executing, by hardware, instructions which belong to a first instruction set and executing, by software, instructions which belong to a second instruction set, said main processor including an interrupt request reception circuit to encode an interrupt vector for said execution of an instruction of said second instruction set by using an interrupt handler, said interrupt request reception circuit generating an interrupt vector address corresponding to said interrupt vector; and a co-processor operative under the control of said main processor autonomously fetching an instruction belonging to said second instruction set to execute same by hardware of said co-processor, said co-processor including an interrupt request generation circuit for decoding an interrupt request signal, said interrupt

request generation circuit being connected to said interrupt request reception circuit by at least one signal line and said decoding allowing said interrupt vector address to be identified in said main processor", as required by claim 1.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-35, all the claims presently pending in the application, are patentably distinct over the prior art of record and that the application is in condition for allowance. The Examiner is respectfully requested to pass the application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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